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DESIGN AND PRODUCTION OF A NEW SURFACE MOUNT CHARGE-INTEGRATING AMPLIFIER FOR CDF

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ABSTRACT

We present our experiences in designing and producing 26,000 new charge-integrating amplifiers for CDF, using surface-mount components. The new amplifiers were needed to instrument 920 new 24-channel CDF RABBIT boards, which are replacing an older design rendered obsolete by increases in the collision rate. Important design considerations were frequency response, physical size and cost.

I. INTRODUCTION

The gas calorimeters of the Fermilab CDF experiment[1] are instrumented with RABBIT system[2] charge-integrating amplifier modules. The modules servicing the plug and forward gas calorimeters[3,4,5] have 24 channels each. These modules can not be used in future experimental operation, because an increase in the collision rate has rendered them obsolete. It consequently became necessary to replace them with an updated version, now called the "GPA" board.

In this paper we discuss the charge integrating amplifier which we have designed and built in large numbers for the new GPA board. The most significant departure from past practice is that the new amplifiers are constructed using surface mount technology (SMT) components mounted onto a finger-sized (.34" tall by 1.6" wide) printed circuit board, with a row of 14 pins along one edge for mounting onto the GPA board. This integrating amplifier will be referred to as the SMT amplifier.

The circuit is a standard folded FET cascode with an extra gain stage, a transistor current source for the FET drain, a simple frequency response compensation circuit and an extra output buffer transistor. Compared to the standard cascode, this amplifier has better power supply rejection, higher gain, higher bandwidth and reasonably good noise figures.

II. REASONS FOR BUILDING THE SMT AMPLIFIERS

A brief discussion of the reasons for building the SMT amplifiers follows. It is felt that this may be of practical interest for those facing similar decisions.

The primary reason for making the SMT amplifiers was to reduce the complexity of having to assemble, debug and maintain several different types of GPA boards. Each of the four CDF gas calorimeter types requires a unique combination of charge gain, integrator input impedance and operating characteristics of certain GPA board functions. The result is that there are 15 different GPA board types. The differences between these are important, and they are difficult to verify visually.

From our previous experiences with board production, it was difficult to imagine how this information could be successfully communicated to an assembly vendor, much less correctly carried out, if the new amplifiers were to be built with through-hole components manually inserted onto the GPA board. It seemed a good idea to assemble the boards in two steps: first the amplifiers, using SMT components placed on little SIP boards, and second, the GPA motherboards, using standard through-hole technology. The number of different objects to be dealt with would only be the sum of the different amplifier types and the different GPA board types, not the product.

It was expected that the tighter layout possible with SMT components and their smaller lead inductances would make it easier to control the amplifier's open-loop response at higher frequencies. However, we had already built systems consisting of 10,000 charge integrating channels based on 800 MHz gain-bandwidth product amplifiers using through-hole components and two-layer printed circuit boards. Therefore, better control of high frequency behavior was an expected benefit, but not a compelling reason for building the SMT amplifiers.

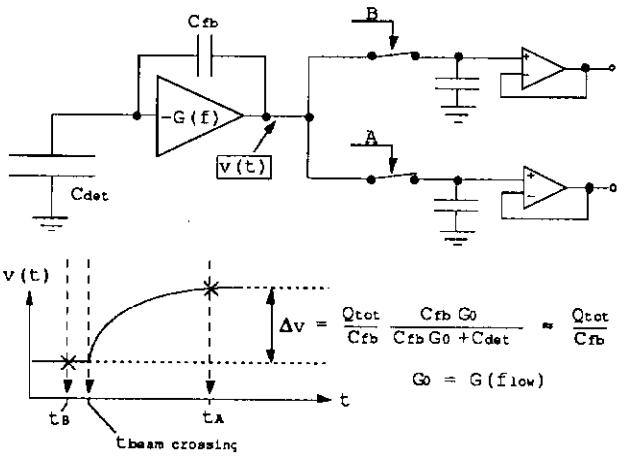

Figure 1. Track-and-hold operation in the RABBIT system.

III. INTEGRATOR OPERATION IN THE RABBIT SYSTEM

In the RABBIT system, charge integrating amplifiers drive two track-and-hold circuits, as shown in Figure 1. Operation of the switches is synchronized with the beam crossings. Just before the beam crossing, at time t_B, switch B is opened to

[1] Operated by the Universities Research Association under contract from the U.S. Department of Energy.

store the integrator output level on capacitor B. Switch A is opened after the beam crossing, with some delay to permit the integrator output to settle. Thus the integrator output swing is stored as the difference between the two voltage levels. An analog pedestal is subtracted from this difference and the result is digitized to 16 bits.

IV. AMPLIFIER DESIGN CONSIDERATIONS

The goals for circuit design were high open-loop gain, high bandwidth, reasonable noise figures, guaranteed stability and low cost. The charge gain (feedback capacitor) values were already known from measurements of the full-scale charges from the detectors.

A. Open-Loop Gain

The low frequency gain, G_0, of a charge integrating amplifier should be sufficiently high that the fraction of available charge collected onto the feedback capacitor is close to 1. The fraction of charge collected is $G_0C_{fb}/(G_0C_{fb}+C_{det})$. For the GPA boards, the largest detector capacitance will be 50 nF, and the corresponding feedback capacitance will be 82 pF. Under the requirement that at least 95% of the available charge should be collected, the amplifier G_0 would have to be 12,000. In our experience, the low frequency gain of the standard FET cascode is about 2000. Therefore the new amplifier would require about 6 times more gain than the standard cascode. The goal was an open-loop gain of at least 10,000.

B. Gain-Bandwidth Product

The gain-bandwidth product (GBW) is determined by the feedback capacitance, C_{fb}, and the desired input impedance, R_{in}, according to the relation:

$$GBW = 1 / (2\pi C_{fb} R_{in}) \ . \qquad (1)$$

Since the characteristic charge collection time is $R_{in}C_{det}$, it is usually desirable to have a small R_{in}, and consequently a large GBW. With very large detectors, however, settling time considerations impose lower limits on the amplifier R_{in}. The capacitance of the detector, the inductance of the interconnecting cables and dynamic amplifier impedance form an underdamped RLC circuit unless $R_{in}>2\sqrt{(L_{cable}/C_{det})}$. After all compromises had been made between collection time and settling time, the amplifier GBW specification was 100 MHz.

C. Noise

Intrinsic amplifier noise is generally a minor concern for CDF gas calorimetry electronics. Detector resolution and environmental noise have always dominated, so careful noise analysis and optimum signal shaping have not been necessary. For most of the components of the CDF detector, intrinsic amplifier noise contributes only a few counts (out of a full scale range of 65,535 counts) to the rms pedestal widths.

D. Cost

Because of the large number of amplifiers to be produced, cost was a significant concern. The goal was to be able to build the amplifiers for less than $5 each.

V. THE CIRCUIT

A. An Overview

The circuit chosen is the boosted gain design shown in Figure 2. The circuit is based on the well-known folded FET cascode, but has some added features: the current source transistor Q2, the gain boosting transistor Q3 and the extra buffer transistor Q6.

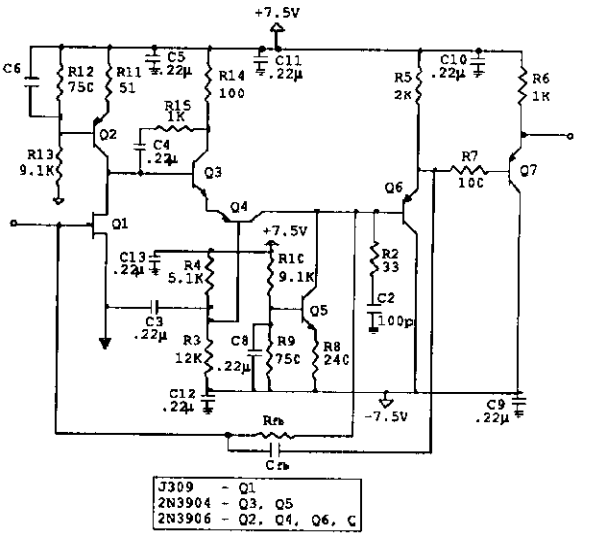

Figure 2. Circuit diagram of the SMT amplifier.

An input signal, ΔV_{in}, applied to the FET gate changes the drain current by $-g_m \cdot \Delta V_{in}$, where g_m is the FET transconductance. This current flows into the base of Q3, where it is boosted by a current gain, β_{eff}, discussed later. The boosted current flows into the low impedance of Q4's emitter and out the collector into the high impedance, Z_{load}, of the amplifying node. The voltage developed here, $Z_{load} \cdot \beta_{eff} \cdot g_m \cdot \Delta V_{in}$, is the amplifier's output signal. For the purposes of this discussion, g_m is independent of frequency, so the gain can be written as

$$G(f) = - g_m \, \beta_{eff}(f) \, Z_{load}(f) \ . \qquad (2)$$

B. Discussion of the Added Features

The current source Q2 is arranged to deliver 10 ma to the FET drain, with perhaps 10 μa diverted into the base of Q3. The current source has the property that the current out of the collector is insensitive to transients in the +7.5 volt power supply voltage. This has been an important consideration in

controlling pedestal drifts in the RABBIT system. Transients tend to occur on the power supply lines when the track-and-hold switches are opened to store the amplifier outputs. In the simplest amplifier designs, there would be just a resistor between the drain and the power supply, so these transients would cause noise in the current delivered to the drain, and consequently noise in the amplifier output. The noise would be part of the amplifier pedestal. Pedestals could then display large drifts, large dependence on the timings of the switch openings, etc. The Q2 current source reduces these effects to insignificance, at the price of adding noise to the amplifier.

Q3 adds gain by amplifying the current signal from Q1. In the absence of the negative feedback circuitry around Q3, it would amplify the current by it's own gain, $\beta(f)$, which would be around 150 at low frequencies. However, the frequency dependence of β would put an additional breakpoint in the overall frequency response. This would occur at the frequency f_T/β_0, where f_T is the transistor's gain-bandwidth product and β_0 is the low frequency gain. The transistor used here has an f_T of around 300 MHz and a β_0 of around 150, so the breakpoint would occur at around 2 MHz. For reasons which will be discussed later, we chose to push this extra breakpoint up in frequency by employing negative feedback around Q3 in order to reduce its effective current gain, β_{eff}, to approximately 8. The added breakpoint in $\beta_{eff}(f)$ should occur at about (300MHz)/8, or 37 MHz, instead of 2 MHz. The factor of 8 extra gain is much better controlled than the transistor's β, and it is comfortably within the desired range of 5 to 10 discussed earlier as the needed extra gain.

Transistors Q4, Q5 and Q6 are standard cascode features. Q4 provides the low impedance path into the amplifying node and sets the operating voltage for the FET. The Q5 current source sets the bias current for Q3 and Q4, and Q6 is the output emitter-follower.

The extra buffer transistor Q7 separates the output from the point where the feedback capacitor is connected. This extra buffer is highly beneficial, because it greatly reduces the track-and-hold switching noise arriving at the amplifier input by way of the feedback capacitor. If Q7 were removed and the track-and-hold switches were driven from Q6's emitter, it could happen that Q6 becomes turned off by the switching noise. If the noise were such as to pull the emitter voltage in the negative direction, Q6 would at first only conduct less. The negative-going disturbance would nevertheless appear at the amplifier input, although attenuated by the detector capacitance. The amplifier would then invert and amplify this, and it would appear as a positive-going disturbance at the base of Q6. By this action, Q6 would become reversed-biased and would turn off.

C. Transistor Choices

The J309 FET was chosen because of good previous experiences. It is relatively inexpensive because it is widely used in other applications. It has moderate gain (gm=.015 mhos at Id=10mA) and consequently a theoretical noise voltage of less than 1 nV/√Hz.

The 2N3904 and 2N3906 were chosen because they are inexpensive, yet adequate for the purpose. One might normally expect the gain boosting transistor Q3 to be a very high f_T device, so that the added roll-off is pushed out to as high a frequency as possible, however the added breakpoint can be compensated for by judicious choices for R_2 and C_2, and it was deemed unnecessary to use faster devices. Reducing the number of different components to be procured and handled helped minimize the cost and complexity of the project. Also, since the highest gain-bandwidth required was 100 MHz, the f_T of Q3 did not have to be greater than 300 MHz.

D. The Frequency Response

Figure 3 shows frequency response curves for this circuit. The curve indicated as "expected response, no compensation" is be the idealized response with R_2 and C_2 removed from the circuit. At low frequencies, the impedance at the amplifying node, $Z_{load}(f=0)$, is the parallel combination of the two collector output impedances, typically $5 \cdot 10^5$ ohms, and the emitter follower input impedance, which is the product of the transistor's β and the corresponding emitter resistor value, or about $6 \cdot 10^5$ ohms. The total impedance should be about $1.7 \cdot 10^5$ ohms. The low frequency gain should then be

$$G_0 = g_m \, \beta_{eff}(f=0) \, Z_{load}(f=0) \, , \qquad (5)$$

or about 20,000. In practice, this number might vary by 50% from amplifier to amplifier. Nevertheless, it amply satisfies the design goal of 10,000 or more.

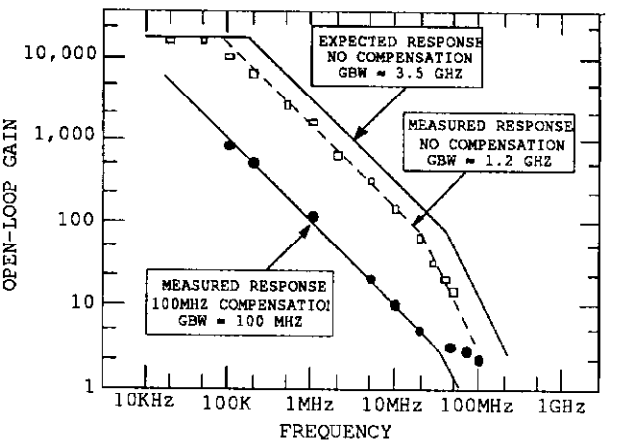

Figure 3. Frequency response.

At about 160 KHz, the parasitic capacitance at the amplifying node (theoretically about 6 pF total) causes $Z_{load}(f)$ to fall with increasing frequency. This 1/f fall-off should continue up to 37 MHz, where $\beta_{eff}(f)$ also will begin to fall as 1/f. The GBW should be (160 KHz)•(20,000) or 3.2 GHz.

The open squares labelled "measured, no compensation" show how one circuit compares with expectations. The GBW is about one-third the expected value. Also, the breakpoint from the gain boosting stage appears to occur at 20 MHz.

The measured GBW far exceeds the design goal of 100 MHz, but such an amplifier would be useless as an integrator because the frequency response has an extra breakpoint at 20 MHz. The integrators would oscillate when connected to detector components having less than about 15 nF source capacitance and would display underdamped ringing for detector capacitances less than about 60 nF.

Resistor R_2 and capacitor C_2 are included to reshape the high frequency load line at the amplifying node. Increasing C_2 reduces the frequency of the first breakpoint. C_2 was chosen to yield a GBW of about 100 MHz. The $\beta_{eff}(f)$ breakpoint can be removed by choosing the appropriate value for R_2. If R_2 is chosen so that its impedance begins to dominate C_2 at the $\beta_{eff}(f)$ breakpoint, then the flattening out of the load line will compensate for the $\beta_{eff}(f)$ roll-off, and should result in an overall frequency response which falls as 1/f.

In practice, the open-loop frequency response often departs somewhat from 1/f dependence in the region above 50 MHz. This causes stability concerns only for detector capacitances which are only a few times larger than the feedback capacitance. For the CDF gas calorimeters, this is of no concern.

E. Noise

We have measured the intrinsic amplifier noise in two ways. The first method was to measure the output power spectral density with a Marconi Instruments model 2382 spectrum analyzer. The second was to read out integrator pedestals through the RABBIT system and to compute rms pedestal widths. In both cases, the source capacitance (C_s) at the amplifier input was varied to allow better identification of the intrinsic amplifier noise.

Figure 4 shows the integrator output noise V_n (in nV/√Hz) vs. C_s, as measured with the spectrum analyzer. The noise power density was measured both at the integrator output and at the circuit ground. The power measurement from ground was subtracted from that at the output. The ground measurement consistently yielded values between 6.6 and 6.7 nV/√Hz.

The integrator feedback capacitance was 150 pF, and the source capacitances were (measured) silvered mica capacitors between 0.46 and 3.34 nF. As C_s is increased, the AC voltage divider between the output and the input becomes more attenuating, causing the amplifier to make larger output changes to correct for the input noise. The output noise should be therefore linear with C_s, with a slope equal to the equivalent input noise voltage, e_n, divided by the integrator feedback capacitance. Also, the offset of this line should be a measure of e_n.

Three different integrators were measured at 1.2 MHz. The output noise is linear with C_s , and the different amplifiers give nearly the same results. Inferred e_n values range from 1.6 to 2.2 nV/√Hz using the offsets of the linear fits, and from 1.5 to 1.6 nV/√Hz using the slopes. It is expected that the slope measurements are more accurate, since the values taken from the offsets can have contributions from other sources, a view consistent with the fact that the e_n values from the offsets are generally higher.

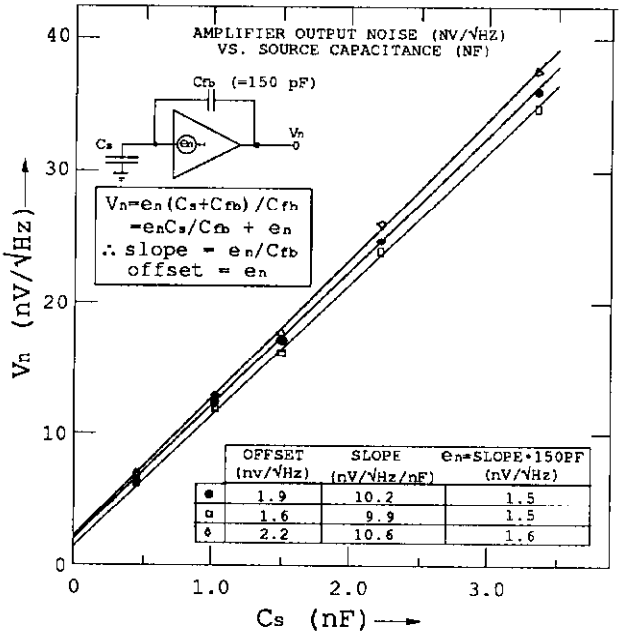

Figure 4. Integrator output noise vs. source capacitance.

These measurements were repeated at 2.5 MHz, with virtually identical results.

Noise measurements were also obtained from the rms widths of pedestal distributions for events as read out through the RABBIT system. Without showing the data or the analysis steps, we simply quote the results: the e_n values are found to range from 1.4 to 1.7 nV/√Hz, in good agreement with the spectrum analyzer results. Expressed in terms of equivalent input noise charge, the rate of increase in noise charge with source capacitance is about 5 femtocoulombs per nanofarad.

VI. PRINTED CIRCUIT LAYOUT

The amplifier board is shown in Figure 5. The resistors and capacitors are standard 1206 packages, and the transistors are SOT-23. The assembly panel contained 70 individual amplifier sections, in a 5 by 14 array. With fiducial marks and tooling holes, the overall panel size was 8" by 10". The panels were fabricated on two layer, 1/32" thick circuit boards.

The circuit layout was complicated by the constraint that the height of the SIP integrator above the GPA board could not exceed .39" . This is RABBIT system requirement. Since the shoulders of the pins would add some height, the board height was limited to 0.34". In the final layout, the 34 components are equally divided between the two sides, and the spacing between components would have to be regarded as tight.

An interesting aspect of the layout is the absence of plated-through holes. In order to minimize fabrication costs, the layout was performed with the constraint that there be no vias, thereby minimizing machining and eliminating a plating step.

Permitting no vias was also important in preserving maximum space for the components. Connections between the two sides are made using the edge pins which were not otherwise necessary for input, output or supplying power.

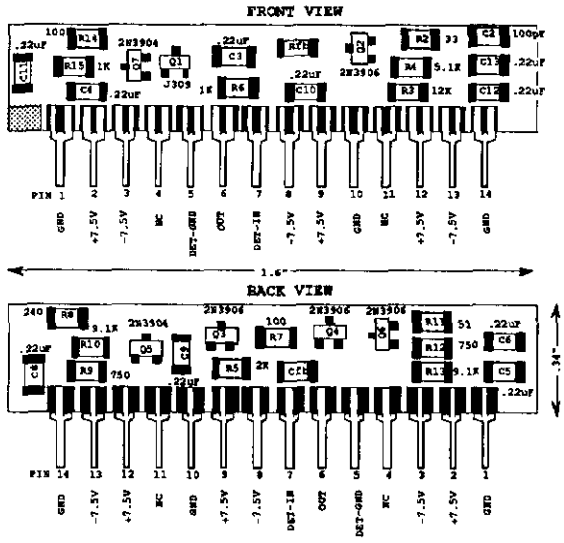

Figure 5. Component layout of the SMT amplifier.

VI. CHECKOUT AND RELIABILITY

GPA board checkout was a three step process which included visual inspection, power checks, power-on burn-in for 8 hours, DC measurements, oscilloscope probing of crucial points, and a comprehensive computerized test and calibration procedure.

The checkout rate was close to 4 boards per man-day. That this is about double the expectation is attributed to the reliability of the SMT amplifiers. The automated process by which the amplifiers were assembled produced a highly uniform product. After initial assembly problems were corrected, the amplifiers were never found to have missing, incorrect or misaligned parts.

Also, amplifiers were tested before being sent to the GPA board assembler. The finished GPA boards were practically guaranteed to have working amplifiers, so the checkout technicians were able to concentrate on problems at the GPA board level. Those few amplifiers found to be bad were just cut away and replaced. Consequently, most of the technicians did not have to be skilled in amplifier problem diagnosis, which would have required a higher level of training.

The yield of good amplifiers from the SMT assembly vendor was about 96.5%. Of the 3.5% which initially failed to work, it was found that most could be easily repaired. The failure modes, in order of decreasing likelihood, were:

(1) broken (cracked) resistors and capacitors,
(2) improper or missing solder connections,
(3) solder bridging, and
(4) failure of individual components.

After installation onto the GPA boards, about 1% of the amplifiers failed. Practically all of these failures occurred during the wave-soldering of the GPA board and were due to either (1) solder erupting up onto the SIP board through the plated-through holes in the GPA board, or (2) solder reflow on the SMT amplifier causing motion of the SMT components.

VI. SUMMARY

Using SIP amplifiers constructed with surface mount components has reduced the complexity involved in producing the 15 different types of the GPA board. Higher than expected amplifier reliability, resulting in an easier checkout task, was an unexpected benefit. The cost per amplifier is $4.71, excluding the labor for engineering and checkout.

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